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(54) **DATA STORAGE DEVICE DETECTING
MEDIA DEFECTS BY WRITING OPPOSITE
POLARITY TEST PATTERN**

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None
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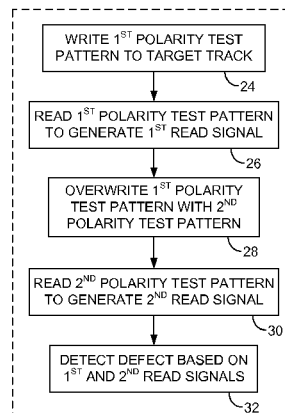
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(57) **ABSTRACT**

A data storage device is disclosed comprising a disk comprising a plurality of tracks, and a head actuated over the disk. A first test pattern having a first polarity is written to a target track, and the first test pattern is read to generate a first read signal. The first test pattern is overwritten with a second test pattern having a second polarity opposite the first polarity, and the second test pattern is read to generate a second read signal. A defect in the target track is detected based on the first read signal and the second read signal.

18 Claims, 4 Drawing Sheets



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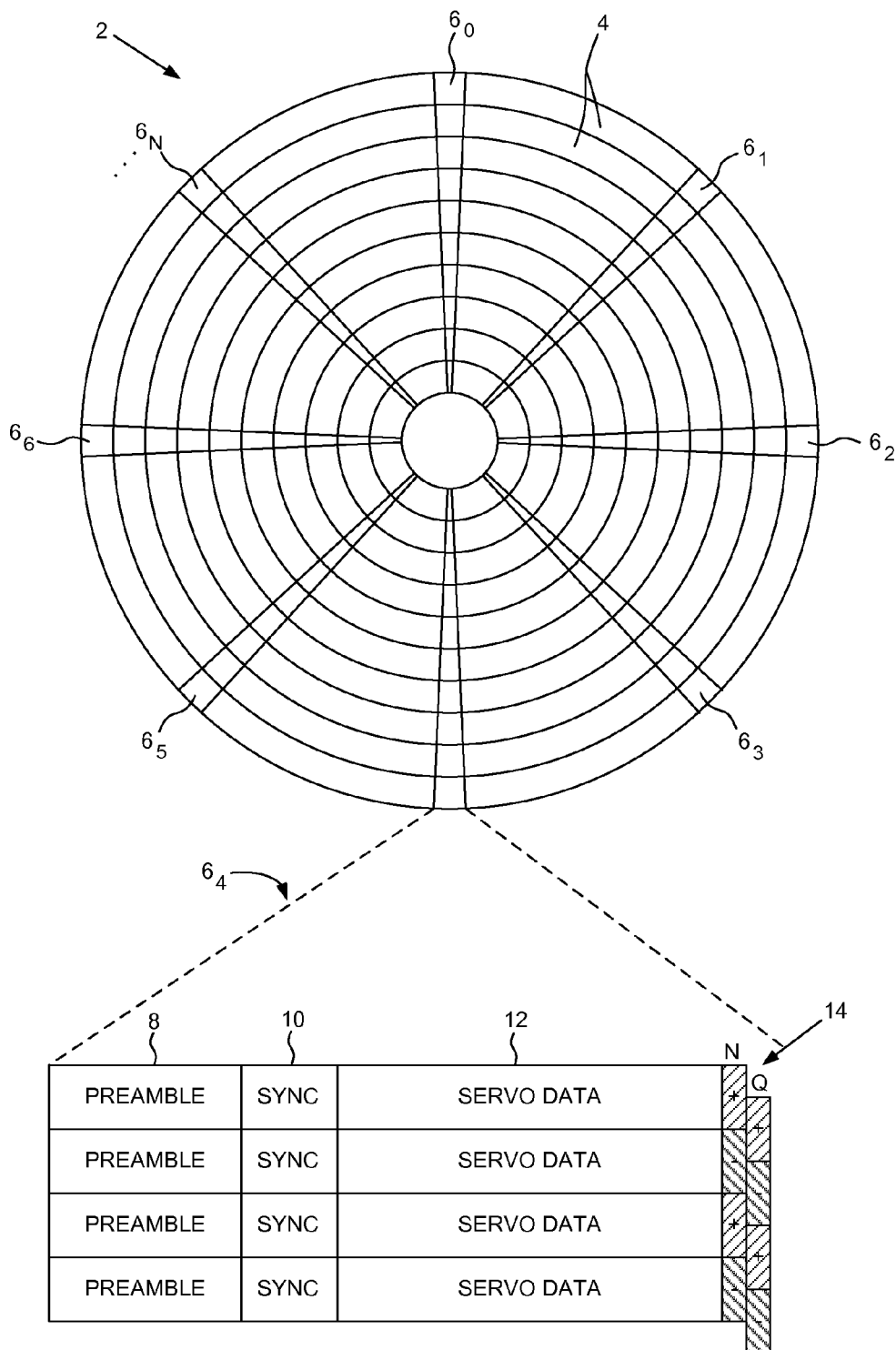


FIG. 1
(Prior Art)

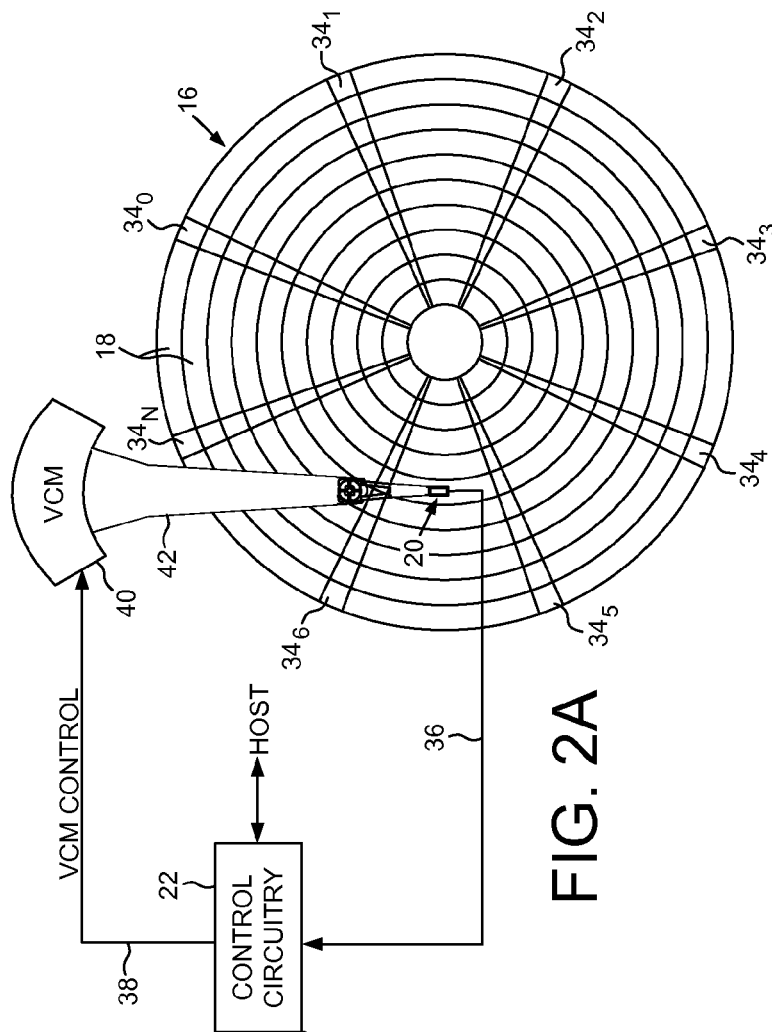


FIG. 2A

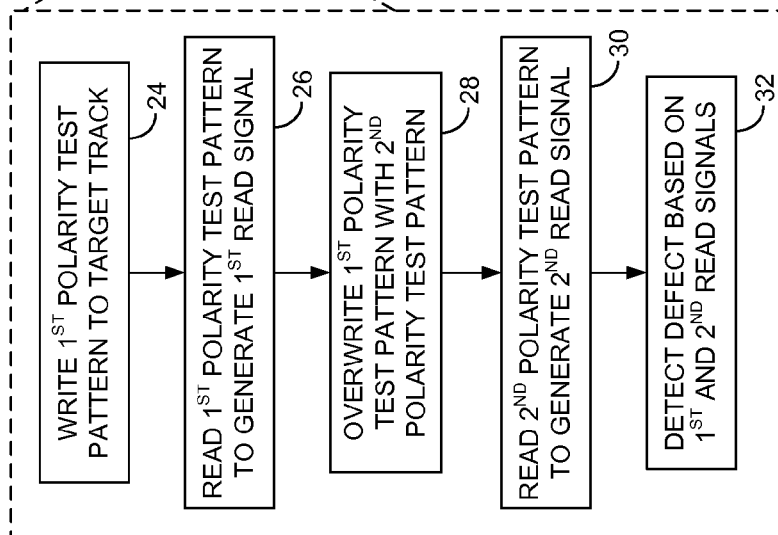


FIG. 2B

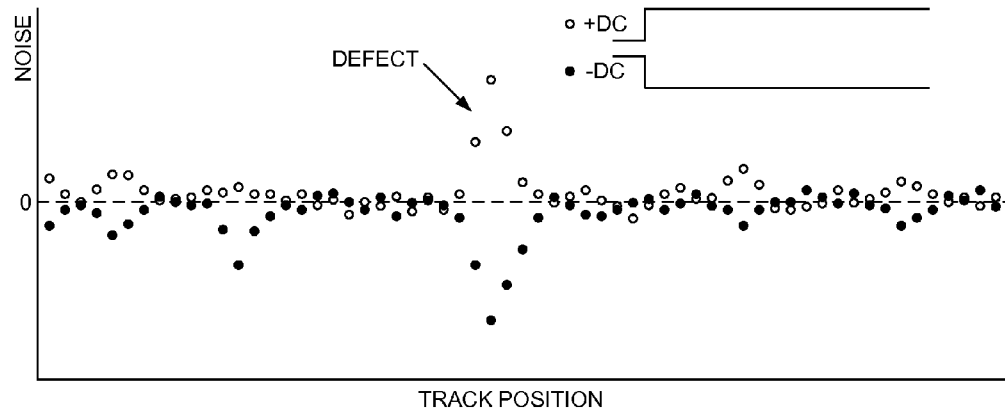


FIG. 3A

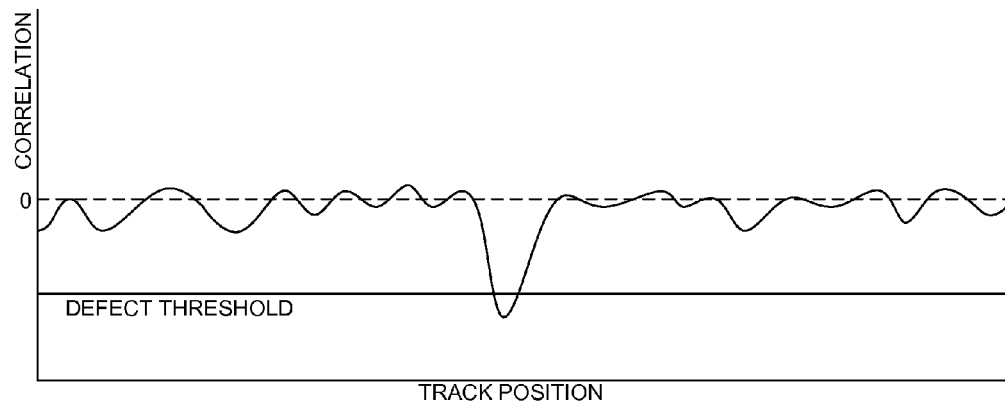


FIG. 3B

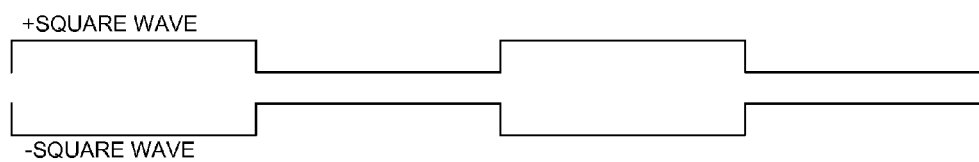


FIG. 4



FIG. 5

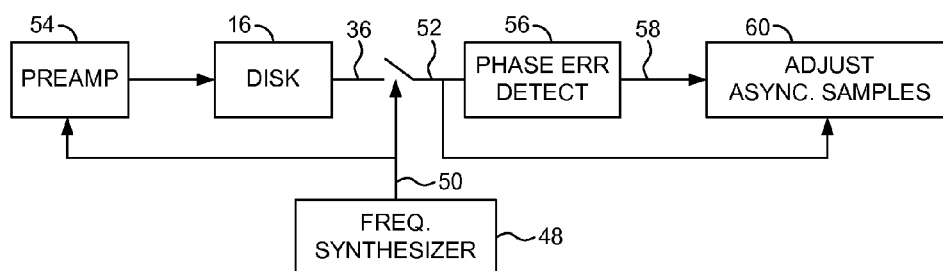


FIG. 6A

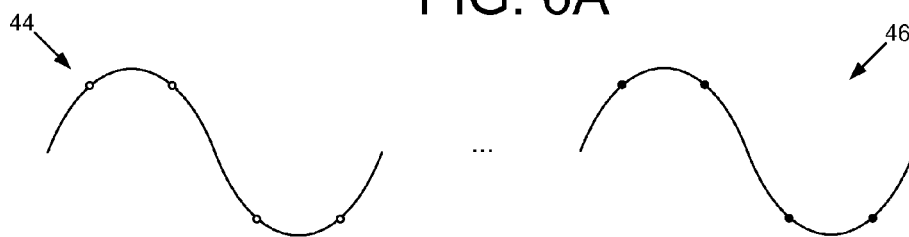


FIG. 6B

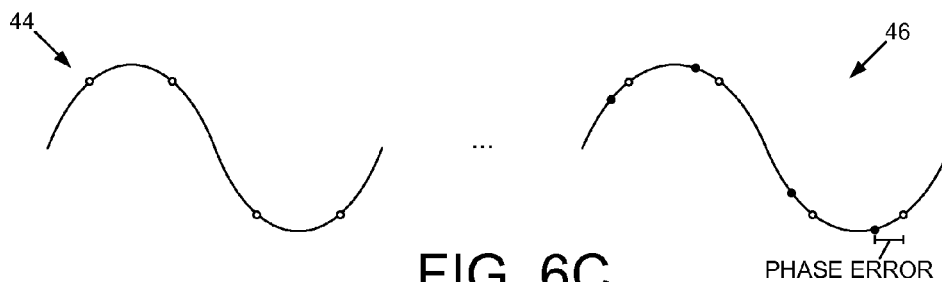


FIG. 6C

1

DATA STORAGE DEVICE DETECTING MEDIA DEFECTS BY WRITING OPPOSITE POLARITY TEST PATTERN

BACKGROUND

Data storage devices such as disk drives comprise a disk and a head connected to a distal end of an actuator arm which is rotated about a pivot by a voice coil motor (VCM) to position the head radially over the disk. The disk comprises a plurality of radially spaced, concentric tracks for recording user data sectors and servo sectors. The servo sectors comprise head positioning information (e.g., a track address) which is read by the head and processed by a servo control system to control the actuator arm as it seeks from track to track.

FIG. 1 shows a prior art disk format 2 as comprising a number of servo tracks 4 defined by servo sectors 6₀-6_N recorded around the circumference of each servo track. Each servo sector 6_i comprises a preamble 8 for storing a periodic pattern, which allows proper gain adjustment and timing synchronization of the read signal, and a sync mark 10 for storing a special pattern used to symbol synchronize to a servo data field 12. The servo data field 12 stores coarse head positioning information, such as a servo track address, used to position the head over a target data track during a seek operation. Each servo sector 6_i further comprises groups of servo bursts 14 (e.g., N and Q servo bursts), which are recorded with a pre-determined phase relative to one another and relative to the servo track centerlines. The phase based servo bursts 14 provide fine head position information used for centerline tracking while accessing a data track during write/read operations. A position error signal (PES) is generated by reading the servo data 12 and servo bursts 14, wherein the PES represents a measured position of the head relative to a centerline of a target servo track. A servo controller processes the PES to generate a control signal applied to a head actuator (e.g., a voice coil motor) in order to actuate the head radially over the disk in a direction that reduces the PES.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 shows a prior art disk format comprising a plurality of tracks defined by servo sectors.

FIG. 2A shows a data storage device in the form of a disk drive comprising a head actuated over a disk.

FIG. 2B is a flow diagram according to an embodiment wherein a defect in a target track is detected by writing a test pattern having a first polarity which is then overwritten with a test pattern having a polarity opposite the first polarity.

FIG. 3A shows an embodiment wherein a positive DC test pattern is written to a target track which is overwritten with a negative DC test pattern.

FIG. 3B shows an embodiment wherein a defect in the target track is detected when a correlation between the first and second read signals exceeds a negative threshold.

FIG. 4 shows an embodiment wherein the test pattern comprises a periodic test pattern in the form of a square wave.

FIG. 5 shows an embodiment wherein the test pattern is written with a preamble and a postamble.

FIG. 6A shows control circuitry according to an embodiment comprising a frequency synthesizer for generating an asynchronous sampling clock, and a phase error detector operable to detect a phase error between the preamble and postamble.

2

FIG. 6B illustrates an example wherein the sampling frequency matches the rotation frequency of the disk, and therefore there is no phase error between the preamble and postamble.

FIG. 6C illustrates an example wherein an error between the sampling frequency and the rotation frequency of the disk results in a phase error between the preamble and postamble.

DETAILED DESCRIPTION

FIG. 2A shows a data storage device in the form of a disk drive according to an embodiment comprising a disk 16 comprising a plurality of tracks 18, and a head 20 actuated over the disk 16. The disk drive further comprises control circuitry 22 configured to execute the flow diagram of FIG. 2B, wherein a first test pattern having a first polarity is written to a target track (block 24), and the first test pattern is read to generate a first read signal (block 26). The first test pattern is overwritten with a second test pattern having a second polarity opposite the first polarity (block 28), and the second test pattern is read to generate a second read signal (block 30). A defect in the target track is detected based on the first read signal and the second read signal (block 32).

In the embodiment of FIG. 2A, the plurality of tracks 18 are defined by servo sectors 34₀-34_N written on the disk 16. In one embodiment, the plurality of tracks 18 comprise a plurality of servo tracks which define data tracks that may be recorded at the same or different radial density, wherein each data track may comprise a number of data sectors. The control circuitry 22 processes a read signal 36 emanating from the head 20 to demodulate the servo sectors 34₀-34_N and generate a position error signal (PES) representing an error between the actual position of the head and a target position relative to a target track. The control circuitry 22 filters the PES using a suitable compensation filter to generate a control signal 38 applied to a voice coil motor (VCM) 40 which rotates an actuator arm 42 about a pivot in order to actuate the head 20 radially over the disk 16 in a direction that reduces the PES. The servo sectors 34₀-34_N may comprise any suitable head position information, such as a track address for coarse positioning and servo bursts for fine positioning. The servo bursts may comprise any suitable pattern, such as an amplitude based servo pattern or a phase based servo pattern.

In one embodiment, the control circuitry 22 may detect defects on the disk 16 for one or more reasons, such as to map out defective data sectors to spare data sectors and/or to evaluate the quality of the recording media in general. In one embodiment, certain types of media defects may manifest as DC noise, particularly the media employed in Heat Assisted Magnetic Recording (HAMR) as compared to other types of media, such as the media employed in Perpendicular Magnetic Recording (PMR). For example, a HAMR media may comprise clusters of grains that may be either un-magnetized or magnetized orthogonal to the surrounding bit cells. In order to detect this type of media defect, in one embodiment a test pattern is written to a target track with a first polarity and then overwritten with an opposite polarity. The resulting read signals (before and after the overwrite) are then evaluated in order to detect a defect caused by DC noise in the media. Any suitable part of the target track may be evaluated, such as by writing the test pattern to a single data sector, multiple data sectors, or one or more segments between the servo sectors 34₀-34_N.

FIG. 3A illustrates an embodiment wherein the test pattern comprises a +DC test pattern and a -DC test pattern. For example, the target track may first be written with the +DC test pattern and then read to generate a first read signal. In the

embodiment of FIG. 3A, the first read signal is sampled to generate first signal samples (represented as white dots). The target track may then be overwritten with the -DC test pattern and then read to generate a second read signal which is sampled to generate second signal samples (represented as black dots). The first signal samples and the second signal samples are then processed to detect a defect, for example, by evaluating a moving window of the signal samples.

FIG. 3A shows an example of how a defect on the disk 16 may manifest in the first and second signal samples. Because the test pattern comprises a DC test pattern, the non-zero amplitude of the signal samples is caused by noise, such as a defect on the disk 16. In the example shown in FIG. 3A, the first and second signal samples generated when reading a defect in the media may comprise an amplitude of opposite polarity due to a DC noise component of the defect. In one embodiment, the defect may be detected based on a correlation of the first and second signal samples. For example, in an embodiment shown in FIG. 3B a defect may be detected when the correlation exceeds a negative threshold. As described above, the correlation may be generated over any suitable length window of the first and second signal samples, and in one embodiment, the correlation may be generated over a number of different length windows in order to detect defects of varying length. Other embodiments may generate any other suitable metric to detect a defect on the disk 16, such by generating a difference between the first and second signal samples and comparing the difference to positive and negative thresholds.

Any suitable test pattern may be written to the target track, including a periodic test pattern as shown in the embodiment of FIG. 4. In the example of FIG. 4, the first test pattern comprises a square wave having a first polarity, and the second test pattern comprises a similar square wave having a polarity opposite the first polarity. Any suitable frequency may be selected for the periodic pattern, wherein in one embodiment the frequency is selected so that the control circuitry 22 may maintain proper timing synchronization as the test pattern is read, thereby enabling accurate timing alignment of the first and second signal samples when searching for defects (e.g., when computing a sliding window correlation between the first and second signal samples). For example, an 8T periodic pattern (where T is a bit cell period) may be employed so that a transition occurs every eighth signal sample, thereby providing the timing information needed to synchronize the signal samples.

In another embodiment, when the test pattern comprises a long sequence between transitions (or no transitions as with a DC test pattern), the control circuitry 22 may write a preamble 44 at the beginning of the test pattern 45 and a postamble 46 at the end of the test pattern 45 as illustrated in FIG. 5 which may be processed in order to synchronize the first signal samples to the second signal samples. This embodiment may be understood with reference to FIG. 6A which shows control circuitry according to an embodiment wherein a frequency synthesizer 48 generates a sampling clock 50 for sampling the read signal 36 asynchronously to generate asynchronous signal samples 52. In one embodiment, the sampling clock 50 is generated at the same frequency used to write the test pattern 45 to the disk 16; that is, the frequency synthesizer 48 applies the sampling clock 50 to a preamp 54 during the write operation so that the test pattern 45 is written to the disk 16 at a target frequency. If when reading the test pattern 45 the disk is rotating at the same frequency as when the test pattern 45 was written, then there will be no frequency error between the sampling clock 50 and the rotation frequency of the disk. Consequently, there will be no phase error

between the signal samples of the preamble 44 and the signal samples of the postamble 46 as illustrated in FIG. 6B. However, if when reading the test pattern 45 the disk is rotating at a different frequency as when the test pattern 45 was written, then the frequency error will induce a phase error between the signal samples of the preamble 44 and the signal samples of the postamble 46 as illustrated in FIG. 6C. Accordingly in the embodiment of FIG. 6A, a phase error detector 56 processes the asynchronous signal samples 52 to detect the phase error 58 between the postamble 46 and the preamble 44. The phase error 58 is then used at block 60 to adjust the asynchronous signal samples representing the test pattern 45 (e.g., using suitable upsampling and/or decimation), thereby compensating for the frequency error between the first and second signal samples representing the first and second polarities of the test pattern.

In one embodiment, the test pattern 45 is read multiple times to generate a plurality of buffered asynchronous signal samples. After adjusting for the frequency error in each of the buffered sequences (and in one embodiment a phase error between the sequences), the sequences are amplitude normalized and averaged to generate a nominal sequence. In one embodiment, this process is repeated for both polarities of the test pattern, and then the resulting nominal sequences of signal samples are evaluated to detect defects.

In the embodiment of FIG. 5, a sync mark 47 may be written following the preamble 44 which is used to detect the beginning of the test pattern 45. In addition, the sync mark 47 in each sequence generated during each read of the test pattern may also be used to coarsely phase align (within a signal sample period) the test pattern signal samples. In one embodiment, since the data may be sampled asynchronously without employing any real-time timing recovery, the sync mark 47 may be recorded as a low frequency, long sequence of bits (e.g., 160 bits) which helps ensure accurate detection of the sync mark 47 within the asynchronous signal samples.

Any suitable control circuitry may be employed to implement the flow diagrams in the above embodiments, such as any suitable integrated circuit or circuits. For example, the control circuitry may be implemented within a read channel integrated circuit, or in a component separate from the read channel, such as a disk controller, or certain operations described above may be performed by a read channel and others by a disk controller. In one embodiment, the read channel and disk controller are implemented as separate integrated circuits, and in an alternative embodiment they are fabricated into a single integrated circuit or system on a chip (SOC). In addition, the control circuitry may include a suitable preamp circuit implemented as a separate integrated circuit, integrated into the read channel or disk controller circuit, or integrated into a SOC.

In one embodiment, the control circuitry comprises a microprocessor executing instructions, the instructions being operable to cause the microprocessor to perform the flow diagrams described herein. The instructions may be stored in any computer-readable medium. In one embodiment, they may be stored on a non-volatile semiconductor memory external to the microprocessor, or integrated with the microprocessor in a SOC. In another embodiment, the instructions are stored on the disk and read into a volatile semiconductor memory when the disk drive is powered on. In yet another embodiment, the control circuitry comprises suitable logic circuitry, such as state machine circuitry.

While the above examples concern a disk drive, the various embodiments are not limited to a disk drive and can be applied to other data storage devices and systems, such as magnetic tape drives, solid state drives, hybrid drives, etc. In addition,

5

some embodiments may include electronic devices such as computing devices, data server devices, media content storage devices, etc. that comprise the storage media and/or control circuitry as described above.

The various features and processes described above may be used independently of one another, or may be combined in various ways. All possible combinations and subcombinations are intended to fall within the scope of this disclosure. In addition, certain method, event or process blocks may be omitted in some implementations. The methods and processes described herein are also not limited to any particular sequence, and the blocks or states relating thereto can be performed in other sequences that are appropriate. For example, described tasks or events may be performed in an order other than that specifically disclosed, or multiple may be combined in a single block or state. The example tasks or events may be performed in serial, in parallel, or in some other manner. Tasks or events may be added to or removed from the disclosed example embodiments. The example systems and components described herein may be configured differently than described. For example, elements may be added to, removed from, or rearranged compared to the disclosed example embodiments.

While certain example embodiments have been described, these embodiments have been presented by way of example only, and are not intended to limit the scope of the inventions disclosed herein. Thus, nothing in the foregoing description is intended to imply that any particular feature, characteristic, step, module, or block is necessary or indispensable. Indeed, the novel methods and systems described herein may be embodied in a variety of other forms; furthermore, various omissions, substitutions and changes in the form of the methods and systems described herein may be made without departing from the spirit of the embodiments disclosed herein.

What is claimed is:

1. A data storage device comprising:
a disk comprising a plurality of tracks;
a head actuated over the disk; and
control circuitry configured to:
write a first test pattern having a first polarity to a target track;
read the first test pattern to generate a first read signal;
overwrite the first test pattern with a second test pattern having a second polarity opposite the first polarity;
read the second test pattern to generate a second read signal; and
detect a defect in the target track based on the first read signal and the second read signal.
2. The data storage device as recited in claim 1, wherein the control circuitry is further configured to:
sample the first read signal to generate first signal samples;
sample the second read signal to generate second signal samples; and
detect the defect in the target track based on the first and second signal samples.
3. The data storage device as recited in claim 2, wherein the control circuitry is further configured to detect the defect in the target track based on a moving window of the first and second signal samples.

6

4. The data storage device as recited in claim 2, wherein the control circuitry is further configured to detect the defect in the target track based on a correlation of the first and second signal samples.

5. The data storage device as recited in claim 4, wherein the control circuitry is further configured to detect the defect in the target track when the correlation exceeds a negative threshold.

6. The data storage device as recited in claim 1, wherein:
the first test pattern comprises a DC test pattern; and
the second test pattern comprises a DC test pattern.

7. The data storage device as recited in claim 1, wherein:
the first test pattern comprises a periodic test pattern; and
the second test pattern comprises a periodic test pattern.

8. The data storage device as recited in claim 1, wherein the defect in the target track increases a DC noise in the first and second read signal.

9. The data storage device as recited in claim 8, wherein the DC noise in the first read signal is opposite in polarity from the DC noise in the second read signal.

10. A method of operating a data storage device, the method comprising:

writing a first test pattern having a first polarity to a target track on a disk;

reading the first test pattern to generate a first read signal;

overwriting the first test pattern with a second test pattern having a second polarity opposite the first polarity;

reading the second test pattern to generate a second read signal; and

detecting a defect in the target track based on the first read signal and the second read signal.

11. The method as recited in claim 10, further comprising:
sampling the first read signal to generate first signal samples;

sampling the second read signal to generate second signal samples; and

detecting the defect in the target track based on the first and second signal samples.

12. The method as recited in claim 11, further comprising detecting the defect in the target track based on a moving window of the first and second signal samples.

13. The method as recited in claim 11, further comprising detecting the defect in the target track based on a correlation of the first and second signal samples.

14. The method as recited in claim 13, further comprising detecting the defect in the target track when the correlation exceeds a negative threshold.

15. The method as recited in claim 10, wherein:
the first test pattern comprises a DC test pattern; and
the second test pattern comprises a DC test pattern.

16. The method as recited in claim 10, wherein:
the first test pattern comprises a periodic test pattern; and
the second test pattern comprises a periodic test pattern.

17. The method as recited in claim 10, wherein the defect in the target track increases a DC noise in the first and second read signal.

18. The method as recited in claim 17, wherein the DC noise in the first read signal is opposite in polarity from the DC noise in the second read signal.

* * * * *